Description

The P9221-R is a high efficiency, Qi-compliant wireless power receiver targeted for applications up to 15W. Using magnetic inductive charging technology, the receiver converts an AC power signal from a resonant tank into a regulated DC output voltage setting with 9V and 12V. The integrated, low RDS (ON) synchronous rectifier and ultra-low dropout offer high efficiency making the product ideally suited for battery-operated applications.

The P9221-R includes an industry-leading 32 bit ARM® Cortex®-M0 processor offering a high level of programmability. In addition, the device features proprietary alignment guide information for optimum coupling between the receiver and the transmitter, a programmable current limit, and a patented over-voltage protection scheme eliminating the need for additional capacitors generally used by the receivers, minimizing the external component count and cost. Together with the P9242-R transmitter (T_X), the P9221-R is a complete wireless power system solution for power applications up to 15W.

The P9221-R is available in a 52-WLCSP package and it is rated for a 0 to 85°C ambient operating temperature range.

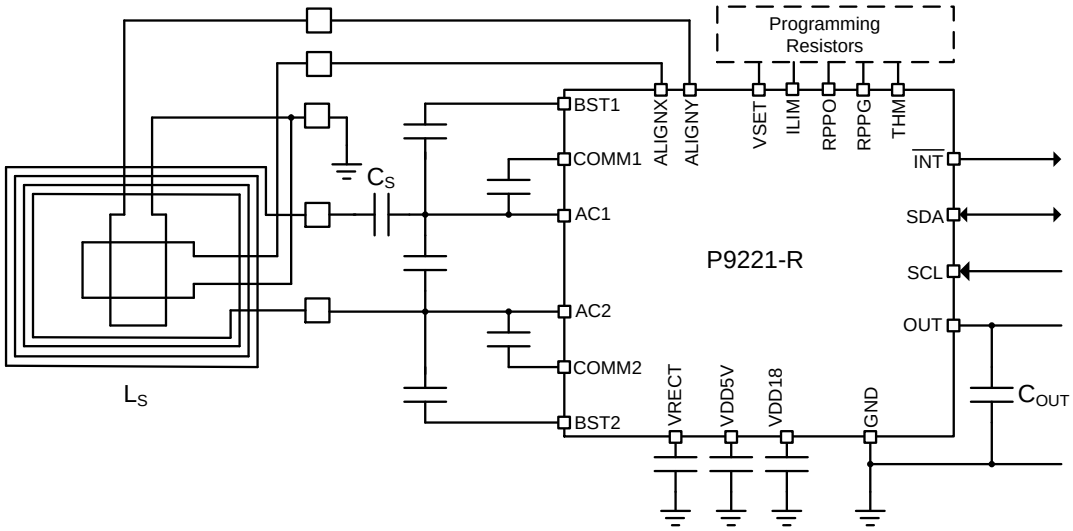
Typical Applications

- Fast charge cellphone
- Tablets
- Accessories
- Medical

Features

- Single-chip solution supporting up to 15W applications
- WPC-1.2.3 compliant
- Patented over-voltage protection clamp eliminating external capacitors
- 87% peak DC-to-DC efficiency with P9242-R T_X
- Proprietary coil alignment guide
- Full synchronous rectifier with low RDS(ON) switches
- Programmable output voltage: 9V and 12V
- Embedded 32-bit ARM® Cortex®-M0 processor
- Dedicated remote temperature sensing
- Power transfer LED indicator
- Programmable current limit
- Active-low enable pin for electrical on/off
- Open-drain interrupt flag
- Supports I^2C interface
- 0 to +85°C ambient operating temperature range
- 52-WLCSP (2.64 × 3.94 mm; 0.4mm pitch)

Typical Application Circuit



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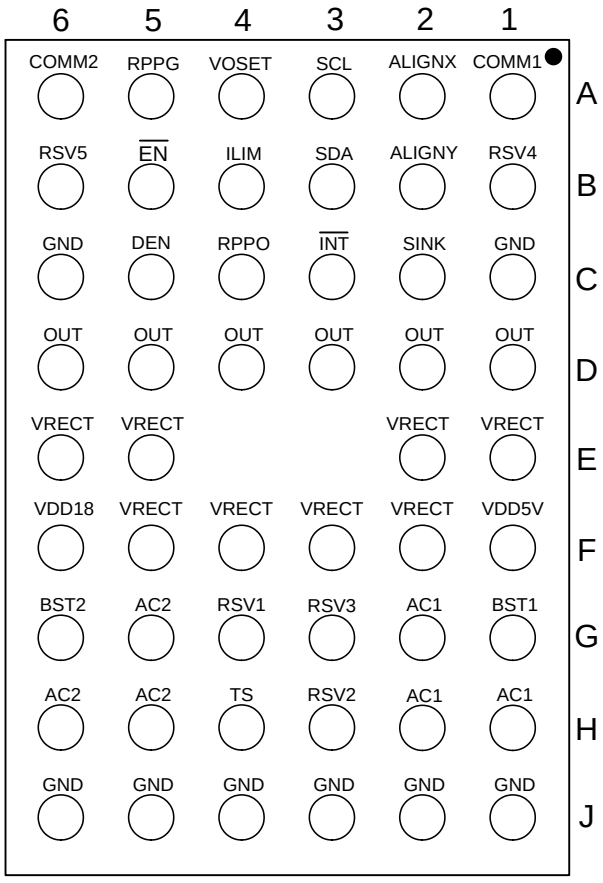
1. Pin Assignments

Figure 1. Pin Assignments



Bottom View

2. Pin Descriptions

Table 1. Pin Descriptions

Pins	Name	Type	Function
A1	COMM1	O	Open-drain output used to communicate with the transmitter. Connect a 47nF capacitor from AC1 to COMM1.
A2	ALIGNX	I	AC input for coil alignment guide. If not used, connect to GND through a 10kΩ resistor.
A3	SCL	I	I²C clock pin. Open-drain output. Connect a 5.1kΩ resistor to VDD18 pin.
A4	VOSET	I	Programming pin for setting the output voltage. Connect this pin to the center tap of a resistor divider to set the output voltage. For more information, refer to section 8.2 for different output voltage settings.

Pins	Name	Type	Function
A5	RPPG	I	Received power packet gain (RPPG) calibration pin for foreign object detection (FOD) tuning. Connect this pin to the center tap of a resistor divider to set the gain of the FOD. The FOD is disabled by connecting the center tap of two 10kΩ resistors to VDD18 pin and GND.
A6	COMM2	O	Open-drain output used to communicate with the transmitter. Connect a 47nF capacitor from AC2 to COMM2.
B1	RSV4		Reserved for internal use. Do not connect.
B2	ALIGNY	I	AC input for coil alignment guide. If not used, connect to GND through a 10KΩ resistor.
B3	SDA	I/O	I²C data pin. Open-drain output. Connect a 5.1 kΩ resistor to VDD18 pin.
B4	ILIM	I	Programmable over-current limit pin. Connect this pin to the center tap of a resistor divider to set the current limit. For more information about the current limit function, see section 8.5.
B5	$\overline{EN}$	I	Active-LOW enable pin. Pulling this pin to logic HIGH forces the device into Shut Down Mode. When connected to logic LOW, the device is enabled. Do not leave this pin floating.
B6	RSV5		Reserved for internal use. Do not connect.
C1, C6, J1, J2, J3,J4,J5,J6	GND	GND	Ground.
C2	SINK	O	Open-drain output for controlling the rectifier clamp. Connect a 36Ω resistor from this pin to the VRECT pin.
C3	$\overline{INT}$	O	Interrupt flag pin. This is an open-drain output that signals fault interrupts. It is pulled LOW if any of these faults exists: an over-voltage is detected, an over-current condition is detected, the die temperature exceeds 140°C, or an external over-temperature condition is detected on the TS pin. It is also asserted LOW when $\overline{EN}$ is HIGH. Connect to VDD18 through a 10kΩ resistor. See section 8.6 for additional conditions affecting the interrupt flag.
C4	RPPO	O	Received power packet offset (RPPO) calibration pin for FOD tuning. Connect to the center tap of the resistor divider to set the offset of the FOD. The FOD is disabled by connecting the center tap of two 10kΩ resistors to VDD18 pin and GND.
C5	DEN	I	Reserved. Must connect a 10kΩ resistor to the VDD18 pin.
D1, D2, D3, D4, D5, D6	OUT	O	Regulated output voltage pin. Connect three 10µF capacitors from this pin to GND. The default voltage is set to 12V when the VOSET pin is pulled up to VDD18 pin through a 10kΩ resister. For more information about VOSET, see section 8.2.
E1, E2, E5, E6 F2, F3, F4, F5	VRECT	O	Output voltage of the synchronous rectifier bridge. Connect three 10µF capacitors from this pin to GND. The rectifier voltage dynamically changes as the load changes. For more information, see the typical waveforms in section 6.
F1	VDD5V	O	Internal 5V regulator output voltage for internal use. Connect a 1µF capacitor from this pin to ground. Do not load the pin.
F6	VDD18	O	Internal 1.8V regulator output voltage. Connect a 1µF capacitor from this pin to ground. Do not load the pin.
G1	BST1	O	Boost capacitor for driving the high-side switch of the internal rectifier. Connect a 15nF capacitor from the AC1 pin to BST1.
G2, H1, H2,	AC1	I	AC input power. Connect to the resonant capacitor (C_S).
G3	RSV3	I	Reserved pins. Must be connected to GND.

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Pins	Name	Type	Function
G4	RSV1		Reserved for internal use. Do not connect.
G5, H5, H6	AC2	I	AC input power. Connect to the Rx coil (L_S).
G6	BST2	O	Boost capacitor for driving the high-side switch of the internal rectifier. Connect a 15nF capacitor from the AC2 pin to BST2.
H3	RSV2		Reserved pins. Must be connected to GND.
H4	TS	I	Remote temperature sensor for over-temperature shutdown. Connect to the NTC thermistor network. If not used, connect to VDD18 pin through the 10kΩ resistor.

3. Absolute Maximum Ratings

Stresses greater than those listed as absolute maximum ratings in Table 2 could cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods might affect reliability.

Table 2. Absolute Maximum Ratings

Pins[a]	Rating[b]	Units
AC1[c], AC2[c], COMM1, COMM2	-0.3 to 20	V
$\overline{EN}$	-0.3 to 28	V
SINK, VRECT	-0.3 to 24	V
DEN, ILIM, RPPG, RPPO, VDD18, VOSET	-0.3 to 2	V
ALIGNX, ALIGNY, $\overline{INT}$, SCL, SDA, TS, VDD5V	-0.3 to 6	V
BST1, BST2	-0.3 to AC1+6, AC2+6	V
OUT	-0.3 to 14.4	V
Maximum Current on SINK	1	A
Maximum RMS Current on COMM1, COMM2	500	mA
Maximum RMS Current from AC1, AC2	2	A

[a] Absolute maximum ratings are not provided for reserved pins (RSV1, RSV2, RSV3, RSV4, RSV5, and DEN). These pins are not used in the application.

[b] All voltages are referred to ground unless otherwise noted.

[c] During synchronous rectifier dead time, the voltage on the AC1 and AC2 pins is developed by current across the power FET's body diodes, and it might be lower than -0.3 V. This is a normal behavior and does not negatively impact the functionality or reliability of the product.

Table 3. ESD Information

Test Model	Pins	Ratings	Units
HBM	All pins except RSV2 and RSV3	2	kV
	RSV2, RSV3 pins	1	kV
CDM	All pins	500	V

4. Thermal Characteristics

Table 4. Package Thermal Information

Note: This thermal rating was calculated on a JEDEC 51 standard 4-layer board with dimensions 76.2 x 114.3 mm in still air conditions.

Symbol	Description	WLCSP Rating 8 Thermal Balls	Units
θ_{JA}	Thermal Resistance Junction to Ambient[a]	47	°C/W
θ_{JC}	Thermal Resistance Junction to Case	0.202	°C/W
θ_{JB}	Thermal Resistance Junction to Board	4.36	°C/W
T_J	Operating Junction Temperature[a]	-5 to +125	°C
T_A	Ambient Operating Temperature[a]	0 to +85	°C
T_{STG}	Storage Temperature	-55 to +150	°C
T_{BUMP}	Maximum Soldering Temperature (Reflow, Pb-Free)	260	°C

[a] The maximum power dissipation is $P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$ where $T_{J(MAX)}$ is 125°C. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the device will enter thermal shutdown.

5. Electrical Characteristics

Table 5. Electrical Characteristics

Note: VRECT = 5.5V; C_{OUT} = 4.7µF, $\overline{EN}$ = LOW, unless otherwise noted. T_J = 0°C to 125°C; typical values are at 25°C.

Symbol	Description	Conditions	Min	Typical	Max	Units
Under-Voltage Lock-Out (UVLO)						
V_{UVLO_Rising}	UVLO Rising	Rising voltage on VRECT		2.9	2.98	V
V_{UVLO_HYS}	UVLO Hysteresis	VRECT falling		200		mV
Over-Voltage Protection						
V_{OVP-DC}	DC Over-Voltage Protection	Rising voltage		13.5		V
$V_{OVP-HYS}$	Over-Voltage Hysteresis			1		V
Quiescent Current						
I_{ACTIVE_SUPLY}	Supply Current	$\overline{EN}$ = Low, No load; VRECT = 12.3V		3.0		mA
I_{SHD}	Shut Down Mode Current	$\overline{EN}$ = High; VRECT = 12.3V		500		µA
VDD18 Voltage						
V_{VDD18}	VDD18 Pin Output Voltage[a]	I_{VDD18} = 10mA, C_{VDD18} = 1µF	1.62	1.8	1.98	V

Symbol	Description	Conditions	Min	Typical	Max	Units
VDD5V Voltage						
V_{VDD5V}	VDD5V Pin Output Voltage [a]	I_{VDD5V} = 10mA, C_{VDD5V} = 1µF	4.5	5	5.5	V
Low Drop-Out (LDO) Regulator						
I_{OUT_MAX}	Maximum Output Current			1.25		A
V_{OUT_12V}	12V Output Voltage	VOSET > 1.5V, VRECT=12.3V		12		V
V_{OUT_9V}	9V Output Voltage	0.7V < VOSET < 1.2V, VRECT=9.3V		9		V
Analog to Digital Converter						
N	Resolution			12		Bit
f_{SAMPLE}	Sampling Rate			67.5		kSa/s
Channel	Number of Channels			8		
$V_{IN,FS}$	Full-Scale Input Voltage			2.1		V
$\overline{EN}$ pin						
V_{IH}	Input Threshold HIGH		1.4			V
V_{IL}	Input Threshold LOW				0.25	V
I_{IL}	Input Current LOW	$V_{\overline{EN}}$ = 0V	-1		1	µA
I_{IH}	Input Current HIGH	$V_{\overline{EN}}$ = 5V		2.5		µA
VOSET, ILIM, TS, RPPO, RPPG						
I_{IL}	Input Current LOW	V_{VOSET}, V_{ILIM}, V_{TS}, V_{RPPO}, V_{RPPG} = 0V	-1		1	µA
I_{IH}	Input Current HIGH	V_{VOSET}, V_{ILIM}, V_{TS}, V_{RPPO}, V_{RPPG} = 1.8V	-1		1	µA
ALIGNX, ALIGNY and $\overline{INT}$ pins						
I_{LKG}	Input Leakage Current	V_{ALIGNX}, V_{ALIGNY}, V_{INT} = 0V and 5V	-1		1	µA
V_{OL}	Output Logic LOW	I_{OL} = 8mA			0.36	V
I²C Interface – SCL, SDA						
V_{IL}	Input Threshold LOW				0.7	V
V_{IH}	Input Threshold HIGH		1.4			V
I_{LKG}	Input Leakage Current	V_{SCL}, V_{SDA} = 0V and 5V	-1		1	µA
V_{OL}	Output Logic LOW	I_{OL} = 8mA			0.36	V
f_{SCL}	Clock Frequency				400	kHz
$t_{HD,STA}$	Hold Time (Repeated) for START Condition		0.6			µs
$t_{HD:DAT}$	Data Hold Time		0			ns
t_{LOW}	Clock Low Period		1.3			µs
t_{HIGH}	Clock High Period		0.6			µs

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Symbol	Description	Conditions	Min	Typical	Max	Units
$t_{SU:STA}$	Set-up Time for Repeated START Condition		0.6			µs
t_{BUF}	Bus Free Time Between STOP and START Condition		1.3			µs
C_B	Capacitive Load for each Bus Line			150		pF
C_I	SCL, SDA Input Capacitance			5		pF
Thermal Shutdown						
T_{SD}	Thermal Shutdown	Rising[b]		140		°C
		Falling		120		°C

[a] Do not externally load. For internal biasing only.

[b] If the die temperature exceeds 130°C, the *Thermal_SHTDN_Status* flag is set and an end power transfer (EPT) packet is sent (see Table 11).

6. Typical Performance Characteristics

The following performance characteristics were taken using a P9242-R, 15 W wireless power transmitter at T_A = 25°C unless otherwise noted.

Figure 2. Efficiency vs. Output Load: V_{OUT} = 12V

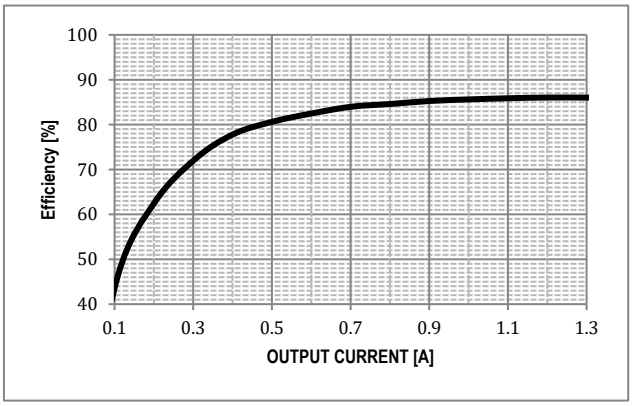


Figure 3. Load Reg. vs. Output Load: V_{OUT} = 12V

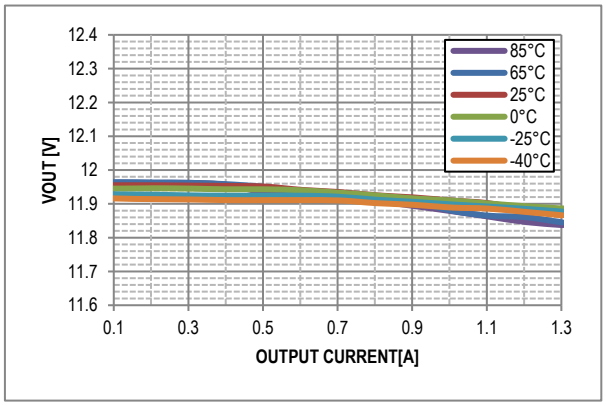


Figure 4. Efficiency vs. Output Load: V_{OUT} = 9V

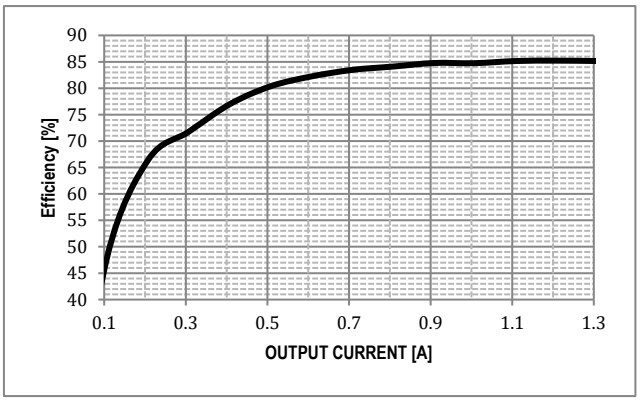


Figure 5. Load Reg. vs. Output Load: V_{OUT} = 9V

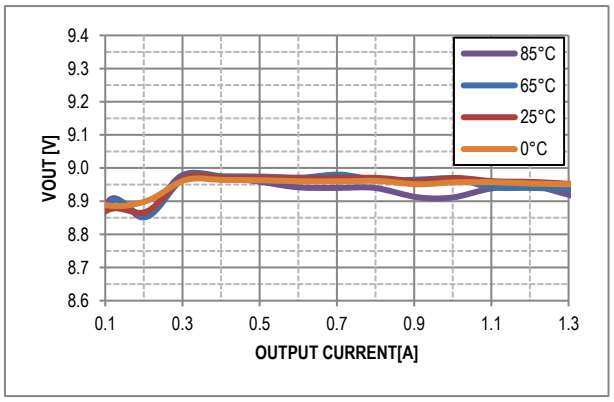


Figure 6. Efficiency vs. Output Load: V_{OUT} = 5V

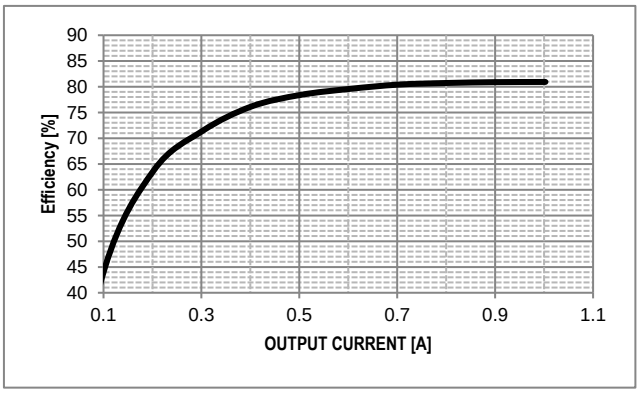


Figure 7. Load Reg. vs. Output Load: V_{OUT} = 5V

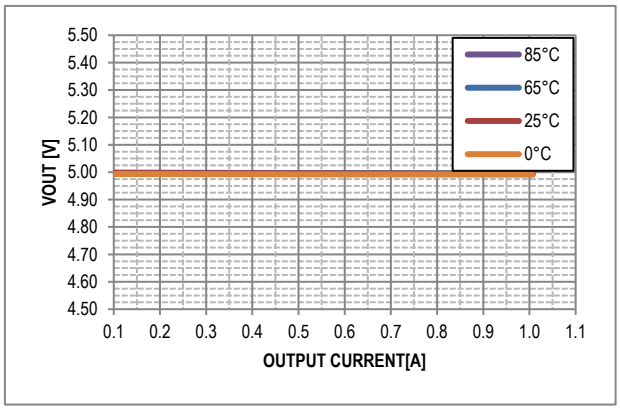


Figure 8. Rectifier Voltage vs. Load: V_{OUT} = 12V

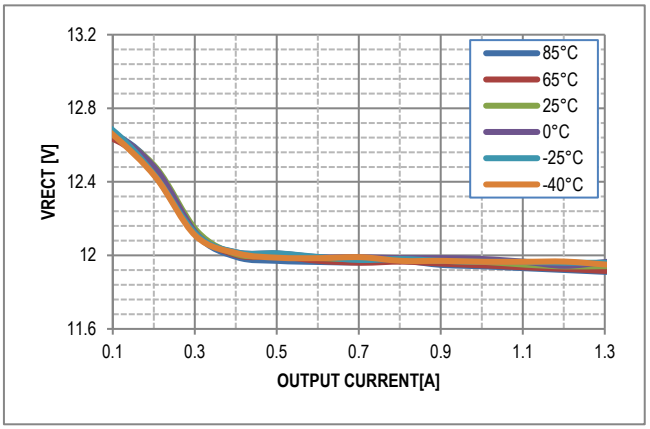


Figure 9. Rectifier Voltage vs. Load: V_{OUT} = 9V

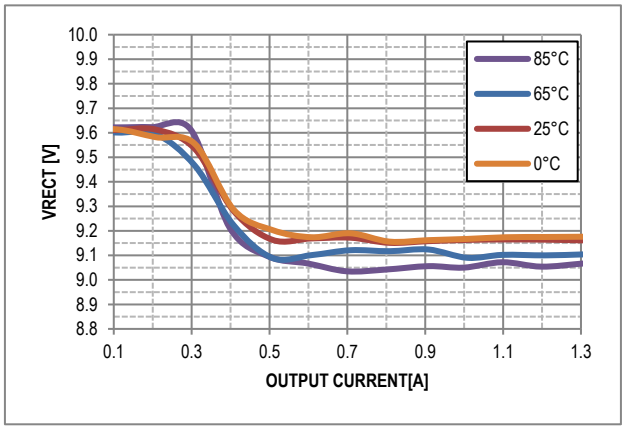


Figure 10. Rectifier Voltage vs. Load: V_{OUT} = 5V

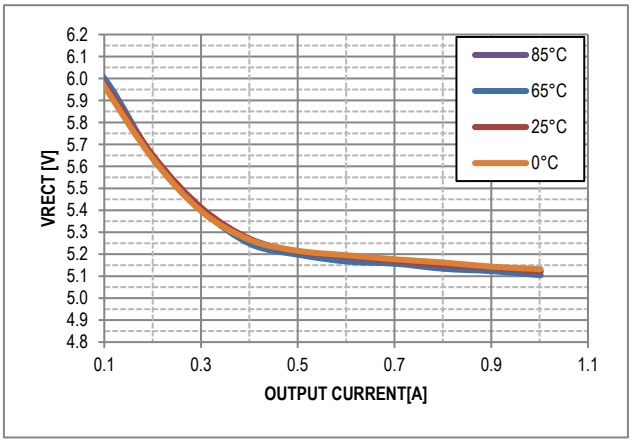


Figure 11. Current Limit vs. V_{ILIM}

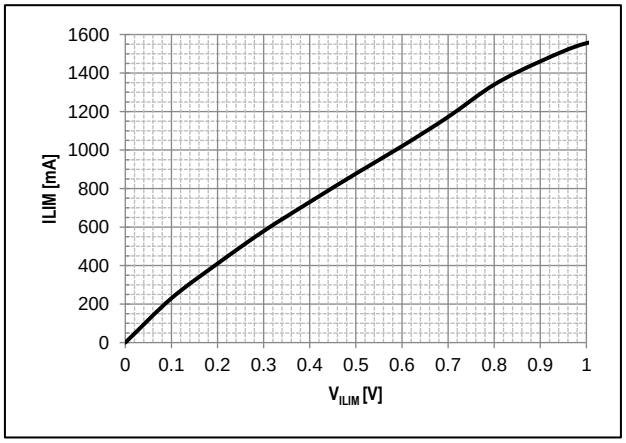


Figure 12. X and Y Misalignment

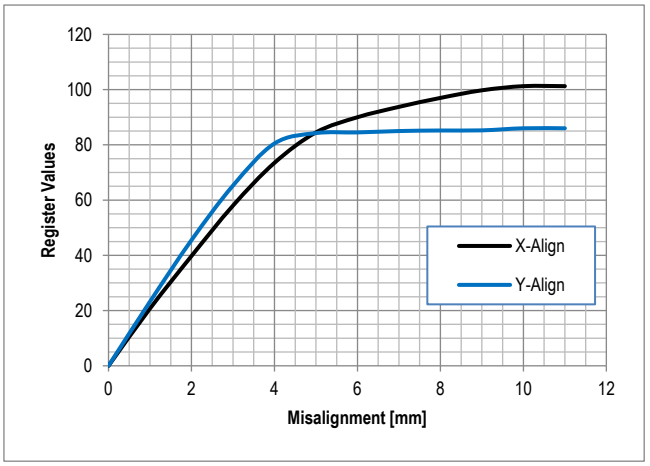


Figure 13. Max. Power vs. Misalignment: V_{OUT}=12V

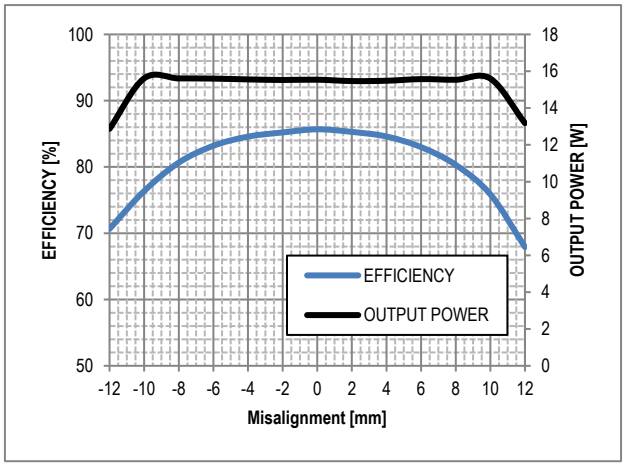


Figure 14. Enable Startup: V_{OUT} = 12V; I_{OUT} = 1.2A

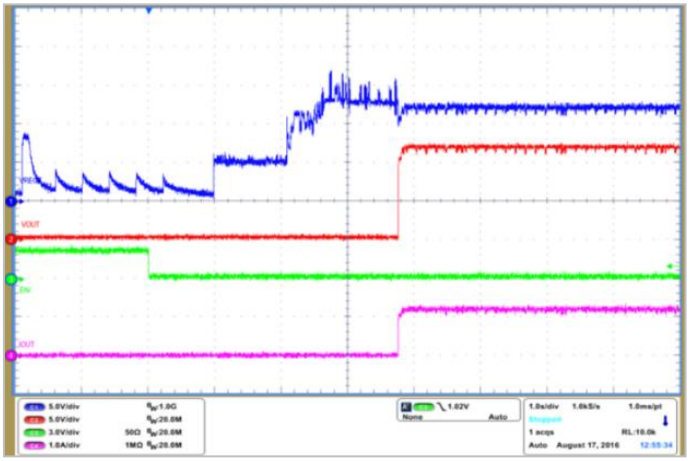


Figure 15. Transient Resp: V_{OUT} = 12V; I_{OUT} = 0 to 1.2A

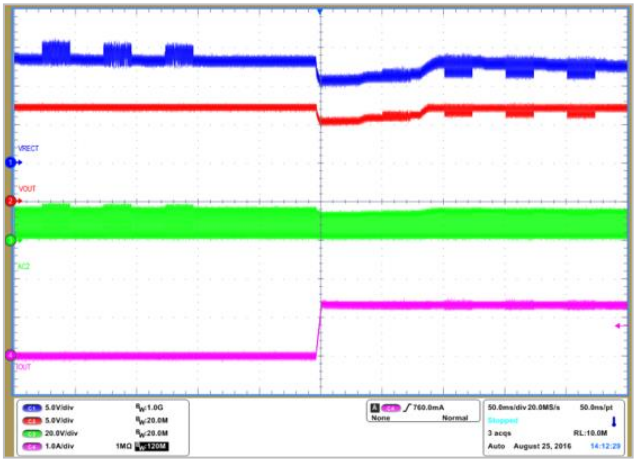
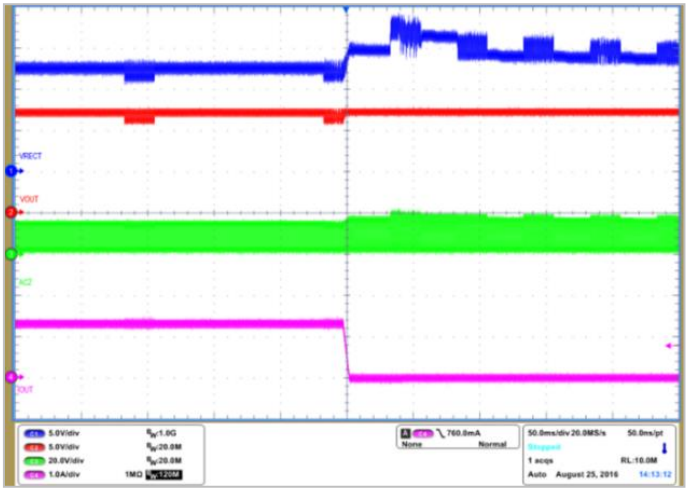
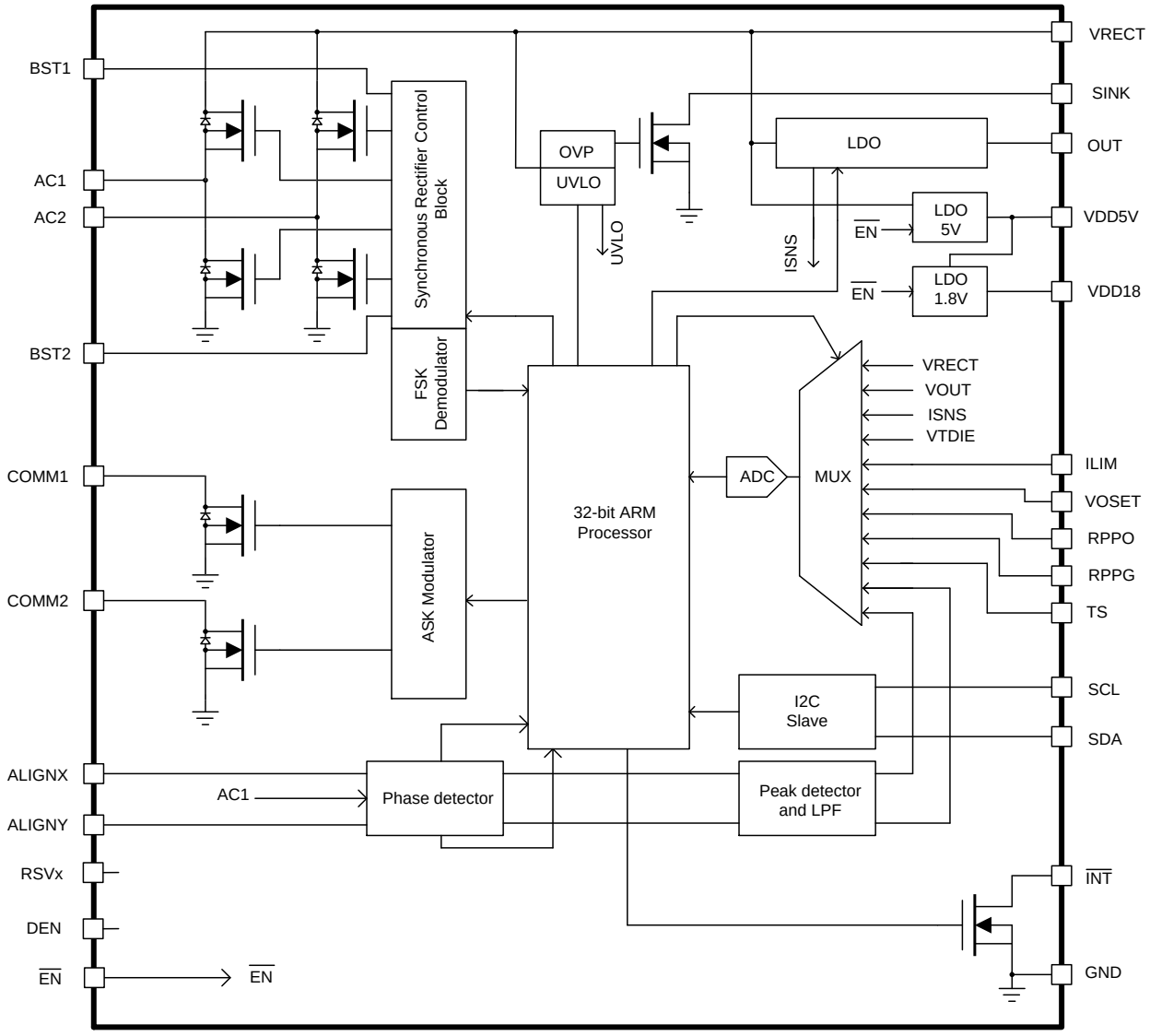


Figure 16. Transient Resp: V_{OUT} = 12V; I_{OUT} = 1.3A to 0



7. Function Block Diagram

Figure 17. Functional Block Diagram



8. Theory of Operation

The P9221-R is a highly-integrated, wireless power receiver targeted for 15W applications. The device integrates a full-wave synchronous rectifier, low-dropout (LDO) linear regulator, and a 32-bit ARM®-based M0 processor to manage all the digital control required to comply with the WPC-1.2.2 communication protocol.

The rectifier voltage and the output current are sampled periodically and digitized by the analog-to-digital converter (ADC). The digital equivalents of the voltage and current are supplied to the internal control logic, which determines whether the loading conditions on the VRECT pin indicate that a change in the operating point is required. If the load is heavy enough and brings the voltage at VRECT below its target, the transmitter is set to a lower frequency that is closer to resonance and to a higher output power. If the voltage at VRECT is higher than its target, the transmitter is instructed to increase its frequency. To maximize efficiency, the voltage at VRECT is programmed to decrease as the LDO's load current increases. The internal temperature is continuously monitored to ensure proper operation.

In the event that the VRECT voltage increases above 13.5V, the control loop disables the LDO and sends error packets to the transmitter in an attempt to bring the rectifier voltage back to a safe operating voltage level while simultaneously clamping the incoming energy using the open-drain SINK pin for VRECT linear clamping. The clamp is released when the VRECT voltage falls below the V_{OVP-DC} minus $V_{OVP-HYS}$. See Figure 17.

The receiver utilizes IDT's proprietary voltage clamping scheme, which limits the maximum voltage at the rectifier pin to 13.5V, reducing the voltage rating on the output capacitors while eliminating the need for over-voltage protection (OVP) capacitors. As a result, it provides a small application area, making it an industry-leading wireless power receiver for high power density applications. Combined with the P9242-R transmitter, the P9221-R is a complete wireless power system solution.

8.1 LDO – Low Dropout Regulators

The P9221-R has three low-dropout linear regulators. The main regulator is used to provide the power required by the battery charger where the output voltage can be set to either 9V or 12V. For more information about setting the output voltage, see section 8.2. It is important to connect a minimum of 30µF ceramic capacitance to the OUT pin.

The other two regulators, VDD5V and VDD18, are to bias the internal circuitry of the receiver. The LDOs must have local 1µF ceramic capacitors placed as close as possible to the pins.

8.2 Setting the Output Voltage – VOSET

The output voltage on the P9221-R is programmed by connecting the center tap of the external resistors R34 and R33 to the VOSET pin as shown in the application schematic in Figure 24. There are only two voltages available: 9.0V or 12V. The recommended settings for R33 and R34 are summarized in Table 6.

The default output voltage is set to 12V in the P9221-R Evaluation Board. For applications where the transmitter is capable of delivering only 5W, the P9221-R will automatically switch to 5V to ensure 5W power delivery. The 5W option can be disabled by adding R33 as described in Table 6.

Table 6. Setting the Output Voltage

R34 (kΩ)	R33 (kΩ)	Output Voltage (V)	5V Output Option
10	OPEN	12	Enable
10	30	12	Disable
OPEN	10	9	Enable
10	3.3	9	Disable

8.3 SINK Pin

The P9221-R has an internal automatic DC clamping to protect the device in the event of high voltage transients. The VRECT node must be connected to the SINK pin at all times using a 36Ω resistor with a greater than ¼ W rating.

8.4 Rectifier Voltage – VRECT

The P9221-R uses a high-efficiency synchronous rectifier to convert the AC signal from the coil to a DC signal on the VRECT pin. During startup, the rectifier operates as a passive diode bridge. Once the voltage on VRECT exceeds the under-voltage lock-out level (UVLO; see Table 5), the rectifier will switch into full synchronous bridge rectifier mode. A total capacitance of 30µF is recommended to minimize the output voltage ripple.

8.5 Over-Current Limit – ILIM

The P9221-R has a programmable current limit function for protecting the device in the event of an over-current or short-circuit fault condition. When the output current exceeds the programmed threshold, the P9221-R will limit the load current by reducing the output voltage. The current limit should be set to 130% of the target maximum output current. See the ILIM pin description in Table 1 for further information.

8.6 Interrupt Function – $\overline{\text{INT}}$

The P9221-R provides an open-drain, active-LOW interrupt output pin. It is asserted LOW when $\overline{\text{EN}}$ is HIGH or any of the following fault conditions have been triggered: the die temperature exceeds 140°C, the external thermistor measurement exceeds the threshold (see section 8.9), or an over-current (OC) or over-voltage (OV) condition is detected.

During normal operation, the $\overline{\text{INT}}$ pin is pulled HIGH. This pin can be connected to the interrupt pin of a microcontroller. The source of the trigger for the interrupt is available in the I²C interrupt register (see Table 12).

8.7 Enable Pin – $\overline{\text{EN}}$

The P9221-R can be disabled by applying a logic HIGH to the $\overline{\text{EN}}$ pin. When the $\overline{\text{EN}}$ pin is pulled HIGH, the device is in Shut Down Mode. Connecting the enable pin to logic LOW activates the device.

8.8 Thermal Protection

The P9221-R integrates thermal shutdown circuitry to prevent damage resulting from excessive thermal stress that may be encountered under fault conditions. This circuitry will shut down or reset the P9221-R if the die temperature exceeds 140°C.

8.9 External Temperature Sensing – TS

The P9221-R has a temperature sensor input, TS, which can be used to monitor an external temperature by using a thermistor. The built-in comparator's reference voltage was chosen to be 0.6V in the P9221-R, and it is used for monitoring the voltage level on the TS pin as described by Equation 1.

$$V_{TS}=V_{VDD18}\times\frac{NTC}{R+NTC}$$ **Equation 1**

Where NTC is the thermistor's resistance and R is the pull-up resistor connected to VDD18 pin. The over–temperature shutdown is trigged when the TS pin voltage is lower than 0.6V; for more information, see Figure 24.

8.10 Alignment Guide – ALIGNX and ALIGNY

This feature is used to provide directional information regarding the transmit coil and receive coil alignment while the wireless charger is in normal operation mode. Sensing coils (see the basic application circuit on the first page) are placed on the wireless power receiver side between the power RX coil and power TX coil. Special design enables the sensing coils to output zero voltage when the alignment is optimum while misalignment between the transmitter and receiver coils will result in a voltage on the sensing coils. These signals are internally rectified, filtered, and passed through the ADC providing quantitative information on the amount of misalignment. The higher the signal is, the more the coils are misaligned.

Furthermore, the signal magnitude on ALIGNX and ALIGNY provides directional information by measuring the phase between the input power AC signal and horizontal and vertical alignment signals. Once the signal passes through the ADC, the alignment information is represented by two 8-bit signed numbers, which can be read from the Alignment X Value and Alignment Y Value I²C registers defined in Table 21 and Table 22 respectively, which indicate the misalignment direction and magnitude.

The application processor can provide 2D visual graphics that suggest how much the power coils are misaligned in each direction and can suggest that the user move the device on the TX pad for the best alignment to improve the power transferred and reduce the charging time.

8.11 Received Power Packet Offset and Gain Calibration – RPPO and RPPG

The received power packet offset (RPPO) and received power packet gain (RPPG) calibrations have dedicated pins for tuning foreign object detection (FOD). The offset calibration can be tuned by the voltage level of RPPO to a value between 0.1V to 2.1V, which corresponds to a power offset range of 1.54W to 2.34W. The gain can be modified by setting the voltage level of the RPPG pin. The range of the control gain is from 0.122 to 2.33 where the level is determined by a ratiometric voltage in the range of 0.1V to 2.1V on the RPPG pin.

To disable the FOD, the voltage on both RPPO and RPPG must be set to 0.1V. Neither pin should be floating. If FOD is not required, the RPPG and RPPO must be set to 0.9V, which defaults to gain = 1 and offset = 0.

8.12 Advanced Foreign Object Detection (FOD)

When metallic objects are exposed to an alternating magnetic field, eddy currents cause such objects to heat up. Examples of such parasitic metal objects are coins, keys, paper clips, etc. The amount of heating depends on the strength of the coupled magnetic field, as well as on the characteristics of the object, such as its resistivity, size, and shape. In a wireless power transfer system, the heating manifests itself as a power loss, and therefore a reduction in power-transfer efficiency. Moreover, if no appropriate measures are taken, the heating could be sufficient that the foreign object could become heated to an undesirable temperature.

During the power transfer phase, the receiver periodically will communicate to the transmitter the amount of power received by means of a received power packet. The transmitter will compare this power with the amount of power transmitted during the same time period. If there is a significant unexplained loss of power, then the transmitter will shut off power delivery because a possible foreign object might be absorbing too much energy.

For a WPC system to perform this function with sufficient accuracy, both the transmitter and receiver must account for and compensate for all of their known losses. Such losses could be due to resistive losses or nearby metals that are part of the transmitter or receiver, etc. Because the system accurately measures its power and accounts for all known losses, it can thereby detect foreign objects because they cause an unknown loss. The WPC specification requires that a power receiver must report to the power transmitter its received power (P_{PR}) in a received-power packet (RPP). The maximum value of the received power accuracy P_{Δ} depends on the maximum power of the power receiver as defined in Table 7.

The power receiver must determine its P_{PR} with an accuracy of $\pm P_{\Delta}$, and report its received power as $P_{RECEIVED} = P_{PR} + P_{\Delta}$. This means that the reported received power is always greater than or equal to the transmitted power (P_{PT}) if there is no foreign object (FO) present on the interface surface.

Table 7. Maximum Estimated Power Loss

Maximum Power [W]	Maximum $P\Delta$ [mW]
15	750

The compensation algorithm includes values that are programmable via either the I²C interface or OTP (one-time programmable) bits. Programmability is necessary so that the calibration settings can be optimized to match the power transfer characteristics of each particular WPC system to include the power losses of the transmit and receive coils, battery, shielding, and case materials under no-load to full-load conditions. The values are based on the comparison of the received power against a reference power curve so that any foreign object can be sensed when the received power is different than the expected system power.

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9. Communication Interface

9.1 Modulation/Communication

The wireless medium power charging system uses two-way communication: receiver-to-transmitter and transmitter-to receiver.

Receiver-to-transmitter communication is accomplished by modulating the load seen by the receiver's inductor; the communication is purely digital and symbols 1's and 0's ride on top of the power signal that exists between the two coils. Modulation is done with amplitude-shift keying (ASK) modulation using internal switches to connect external capacitors from AC1 and AC2 to ground (see Figure 17) with a bit rate of 2Kbps. To the transmitter, this appears as an impedance change, which results in measurable variations of the transmitter's output waveform. The power transmitter detects this as a modulation of coil current/voltage to receive the packets.

Transmitter-to-receiver communication is accomplished by frequency-shift keying (FSK) modulation over the power signal frequency. The power receiver P9221-R has the means to demodulate FSK data from the power signal frequency and use it in order to establish the handshaking protocol with the power transmitter.

The P9221-R implements FSK communication when used in conjunction with WPC-compliant transmitters, such as the P9242-R. The FSK communication protocol allows the transmitter to send data to the receiver using the power transfer link in the form of modulating the power transfer signal. This modulation appears in the form of a change in the base operating frequency (f_{OP}) to the modulated operating frequency (f_{MOD}) in periods of 256 consecutive cycles. Equation 2 should be used to compute the modulated frequency based on any given operating frequency. The P9221-R will only implement positive FSK polarity adjustments; in other words, the modulated frequency will always be higher than the operating frequency during FSK communication.

Communication packets are transmitted from transmitter to receiver with less than 1% positive frequency deviation following any receiver-to-transmitter communication packet. The frequency deviation is calculated using Equation 2.

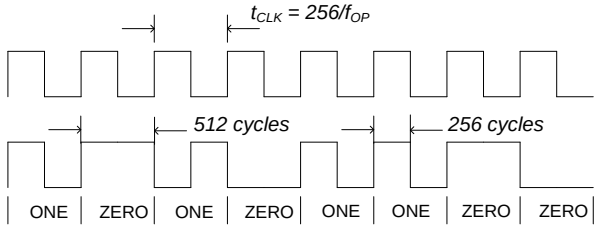
$$f_{MOD} = \frac{60000}{\frac{60000}{f_{OP}} - 3} \ [KHz]$$

Equation 2

Where f_{MOD} is the changed frequency in the power signal frequency; f_{OP} is the base operating frequency of the power transfer; and 60000kHz is the internal oscillator responsible for counting the period of the power transfer signal.

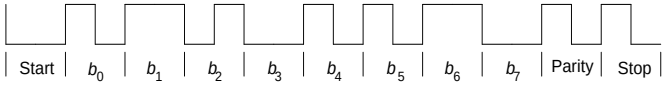
The FSK byte-encoding scheme and packet structure comply with the WPC specification revision 1.2.2. The FSK communication uses a bi-phase encoding scheme to modulate data bits into the power transfer signal. The start bit will consist of 512 consecutive f_{MOD} cycles (or logic '0'). A logic '1' value will be sent by sending 256 consecutive f_{OP} cycles followed by 256 f_{MOD} cycles or vice versa, and a logic '0' is sent by sending 512 consecutive f_{MOD} or f_{OP} cycles.

Figure 18. Example of Differential Bi-phase Decoding for FSK



Each byte will comply with the start, data, parity, and stop asynchronous serial format structure shown in Figure 19:

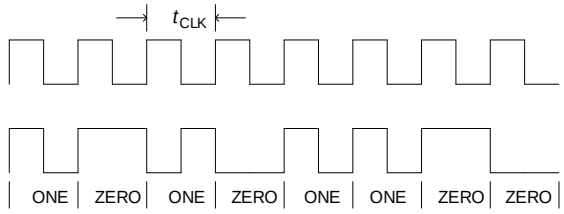
Figure 19. Example of Asynchronous Serial Byte Format for FSK



9.2 Bit Encoding Scheme for ASK

As required by the WPC, the P9221-R uses a differential bi-phase encoding scheme to modulate data bits onto the power signal. A clock frequency of 2kHz is used for this purpose. A logic ONE bit is encoded using two narrow transitions, whereas a logic ZERO bit is encoded using one wider transition as shown below:

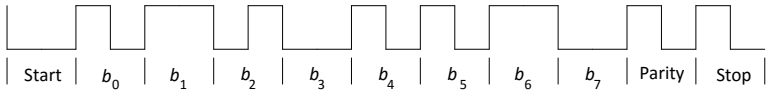
Figure 20. Bit Encoding Scheme



9.3 Byte Encoding for ASK

Each byte in the communication packet comprises 11 bits in an asynchronous serial format, as shown in Figure 21.

Figure 21. Byte Encoding Scheme



Each byte has a start bit, 8 data bits, a parity bit, and a single stop bit.

9.4 Packet Structure

The P9221-R communicates with the base station via communication packets. Each communication packet has the following structure:

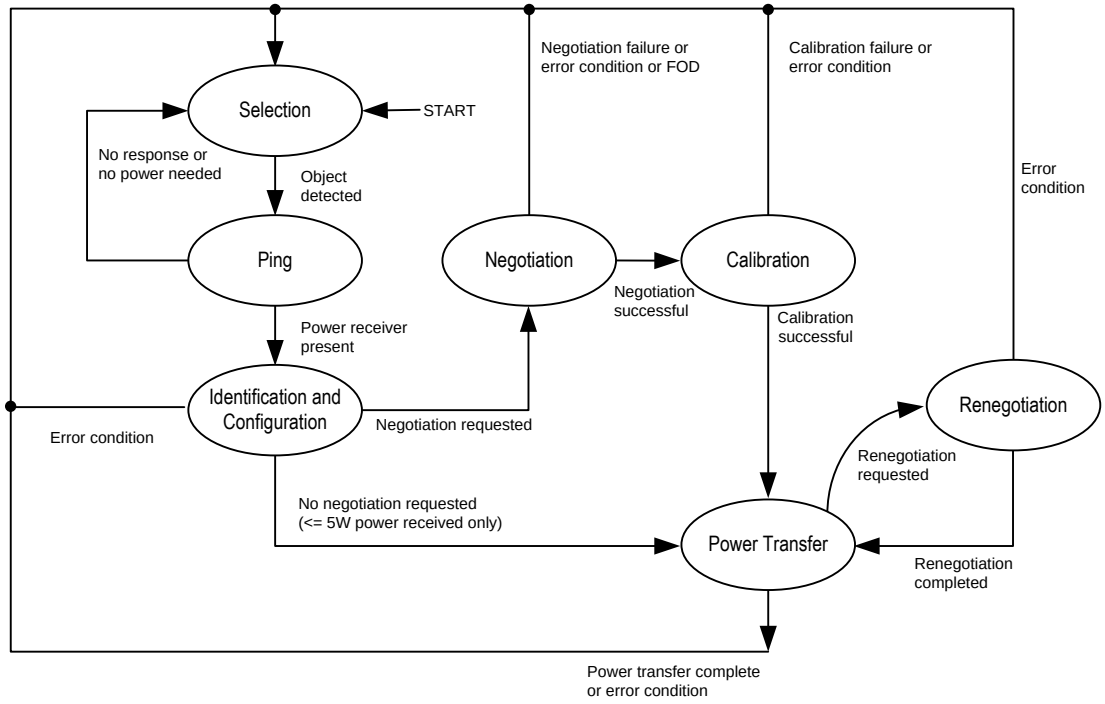
Figure 22. Communication Packet Structure

Preamble	Header	Message	Checksum

10. WPC Mode Characteristics

The Extended Power Profile adds a negotiation phase, a calibration phase, and renegotiation phase to the basic system control functionality of the Base line Power Profile, as shown in Figure 23.

Figure 23. WPC Power Transfer Phases Flowchart



10.1 Selection Phase or Startup

In the selection phase, the power transmitter determines if it will proceed to the ping phase after detecting the placement of an object. In this phase, the power transmitter typically monitors the interface surface for the placement and removal of objects using a small measurement signal. This measurement signal should not wake up a power receiver that is positioned on the interface surface.

10.2 Ping Phase (Digital Ping)

In the ping phase, the power transmitter will transmit power and will detect the response from a possible power receiver. This response ensures the power transmitter that it is dealing with a power receiver rather than some unknown object. When a mobile device containing the P9221-R is placed on a WPC “Qi” charging pad, it responds to the application of a power signal by rectifying this power signal. When the voltage on VRECT is greater than the UVLO threshold, then the internal bandgaps, reference voltage, and the internal voltage regulators (5V and 1.8V) are turned on, and microcontroller’s startup is initiated enabling the WPC communication protocol.

If the power transmitter correctly receives a signal strength packet, the power transmitter proceeds to the identification and configuration phase of the power transfer, maintaining the power signal output.

10.3 Identification and Configuration Phase

The identification and configuration phase is the part of the protocol that the power transmitter executes in order to identify the power receiver and establish a default power transfer contract. This protocol extends the digital ping in order to enable the power receiver to communicate the relevant information.

In this phase, the power receiver identifies itself and provides information for a default power transfer contract:

- It sends the configuration packet.
- If the power transmitter does not acknowledge the request (does not transmit FSK modulation), the power receiver will assume 5W output power.

10.4 Negotiation Phase

In the negotiation phase, the power receiver negotiates changes to the default power transfer contract. In addition, the power receiver verifies that the power transmitter has not detected a foreign object.

10.5 Calibration Phase

In the calibration phase, the power receiver provides information that the power transmitter can use to improve its ability to detect foreign objects during power transfer.

10.6 Power Transfer Phase

In this phase, the P9221-R controls the power transfer by means of the following control data packets:

- Control Error Packets
- Received Power Packet (RPP, FOD related)
- End Power Transfer (EPT) Packet

Once the “identification and configuration” phase is completed, the transmitter initiates the power transfer mode. The P9221-R control circuit measures the rectifier voltage and sends error packets to the transmitter to adjust the rectifier voltage to the level required to maximize the efficiency of the linear regulator and to send to the transmitter the actual received power packet for foreign object detection (FOD) to guarantee safe, efficient power transfer.

In the event of an EPT issued by the application, the P9221-R turns off the LDO and continuously sends EPT packets until the transmitter removes the power and the rectified voltage on the receiver side drops below the UVLO threshold.

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11. Functional Registers

The following tables provide the address locations, field names, available operations (R or RW), default values, and functional descriptions of all the internally accessible registers contained within the P9221-R. The default I²C slave address is 61_{HEX}.

Table 8. Device Identification Register

Address and Bit	Register Field Name	R/W	Default	Function and Description
00_{HEX} [7:0]	Part_number_L	R	20_{HEX}	Chip ID low byte
01_{HEX} [7:0]	Part_number_H	R	92_{HEX}	Chip ID high byte

Table 9. Firmware Major Revision

Address and Bit	Register Field Name	R/W	Default	Function and Description
04_{HEX} [7:0]	FW_Major_Rev_L	R	01_{HEX}	Major firmware revision low byte
05_{HEX} [7:0]	FW_Major_Rev_H	R	00_{HEX}	Major firmware revision high byte

Table 10. Firmware Minor Revision

Address and Bit	Register Field Name	R/W	Default	Function and Description
06_{HEX} [7:0]	FW_Minor_Rev_L	R	26_{HEX}	Minor firmware revision low byte
07_{HEX} [7:0]	FW_Minor_Rev_H	R	04_{HEX}	Minor firmware revision high byte

Table 11. Status Registers

Address and Bit	Register Field Name	R/W	Default	Function and Description
34_{HEX} [7]	Vout_Status	R	0_{BIN}	"0" output voltage is off. "1" output voltage is on.
34_{HEX} [6]	Reserved	R	0_{BIN}	
34_{HEX} [5]	Reserved	R	0_{BIN}	
34_{HEX} [4]	Reserved	R	0_{BIN}	
34_{HEX} [3]	Reserved	R	0_{BIN}	
34_{HEX} [2]	Thermal_SHTDN_Status	R	0_{BIN}	"0" indicates no over-temperature condition exists. "1" indicates that die temperature exceeds 130°C or NTC is less than 0.6V. The P9221-R sends an end power transfer (EPT) packet to the transmitter.
34_{HEX} [1]	VRECT_OV_ Status	R	0_{BIN}	"1" indicates rectifier exceeds 20V for V_{OUT}=12. EPT packet send.
34_{HEX} [0]	Current_Limit_Status	R	0_{BIN}	"1" indicates current limit has been exceeded. The P9221-R sends an end power transfer (EPT) packet to the transmitter.
35_{HEX} [7:0]	Reserved	R	00_{HEX}	

Table 12. Interrupt Status Registers

Address and Bit	Register Field Name	R/W	Default	Function and Description
36_{HEX} [7]	INT_Vout_Status	R	0_{BIN}	"0" output voltage has not changed. "1" output voltage changed.
36_{HEX} [6]	Reserved	R	0_{BIN}	
36_{HEX} [5]	Reserved	R	0_{BIN}	
36_{HEX} [4]	Reserved	R	0_{BIN}	
36_{HEX} [3]	Reserved	R	0_{BIN}	
36_{HEX} [2]	INT_OVER_TEMP_Status	R	0_{BIN}	"1" indicates over-temperature condition exists.
36_{HEX} [1]	INT_VRECT_OV_ Status	R	0_{BIN}	"1" indicates rectifier over-voltage condition exists.
36_{HEX} [0]	INT_OC_Limit_Status	R	0	"1" indicates current limit has been exceeded.
37_{HEX} [7:0]	Reserved	R	00_{HEX}	

Note: If any bit in the *Interrupt Status* register 36_{HEX} is "1" and the corresponding bit in the *Interrupt Enable* register 38_{HEX} is set to "1", the $\overline{INT}$ pin will be pulled down indicating an interrupt event has occurred.

Table 13. Interrupt Enable Registers

Address and Bit	Register Field Name	R/W	Default	Function and Description
38_{HEX} [7]	Vout_CHGN_INTR_EN	RW	0_{BIN}	"0" disables the interrupt. "1" enables the interrupt.
38_{HEX} [6]	Reserved	R	0_{BIN}	
38_{HEX} [5]	Reserved	R	0_{BIN}	
38_{HEX} [4]	Reserved	R	1_{BIN}	
38_{HEX} [3]	Reserved	R	0_{BIN}	
38_{HEX} [2]	OVER_TEMP_INT_EN	R	0_{BIN}	"0" disables the interrupt. "1" enables the interrupt.
38_{HEX} [1]	VRECT_OV_INT_EN	RW	0_{BIN}	"0" disables the interrupt. "1" enables the interrupt.
38_{HEX} [0]	OC_Limit_INT_EN	RW	0_{BIN}	"0" disables the interrupt. "1" enables the interrupt.
39_{HEX} [7:0]	Reserved	RW	00_{HEX}	

Table 14. Battery Charge Status

Address and Bit	Register Field Name	R/W	Default	Function and Description
$3A_{HEX}$ [7:0]	Batt_Charg_status	R/W	00_{HEX}	Battery charge status value sent to transmitter.[a]

[a] Firmware only forwards the data from the application processor to transmitter.

Table 15. End Power Transfer

The application processor initiates the end power transfer (EPT).

Address and Bit	Register Field Name	R/W	Default	Function and Description
$3B_{HEX}$ [7:0]	EPT_Code	R/W	00_{HEX}	EPT_Code sent to transmitter.

Table 16. Read Register – Output Voltage

$$VOUT = \frac{ADC\_VOUT * 6 * 2.1}{4095}$$

Address and Bit	Register Field Name	R/W	Default	Function and Description
$3C_{HEX}$ [7:0]	ADC_VOUT [7:0]	R	00_{HEX}	8 LSB of VOUT ADC value.
$3D_{HEX}$ [7:4]	Reserved	R	0_{HEX}	Reserved.
$3D_{HEX}$ [3:0]	ADC_VOUT [11:8]	R	0_{HEX}	4 MSB of VOUT ADC value.

Table 17. Read Register – VRECT Voltage

$$VRECT = \frac{ADC\_VRECT * 10 * 2.1}{4095}$$

Address and Bit	Register Field Name	R/W	Default	Function and Description
40_{HEX} [7:0]	ADC_VRECT [7:0]	R	–	8 LSB of VRECT ADC value.
41_{HEX} [7:4]	Reserved	R	0_{HEX}	Reserved
41_{HEX} [3:0]	ADC_VRECT [11:8]	R	–	4 MSB of VRECT ADC value.

Table 18. Read Register – IOUT Current

$$IOUT = \frac{RX\_IOUT * 2 * 2.1}{4095}$$

Address and Bit	Register Field Name	R/W	Default	Function and Description
44_{HEX} [7:0]	RX_IOUT [7:0]	R_{HEX}	–	8 LSB of IOUT. Output current in mA.
45_{HEX} [7:0]	RX_IOUT [15:8]	R_{HEX}	–	8 MSB of IOUT. Output current in mA

Table 19. Read Register – Die Temperature

$T_{DIE}=(ADC\_Die\_Temp - 1350)\frac{83}{444} - 273$ where ADC_Die_Temp = 12 bits from ADC_Die_Temp_H and ADC_Die_Temp_L.

Address and Bit	Register Field Name	R/W	Default	Function and Description
46_{HEX} [7:0]	ADC_Die_Temp_L	R	-	8 LSB of current die temperature in °C.
47_{HEX} [7:4]	Reserved	R	0_{HEX}	Reserved
47_{HEX} [3:0]	ADC_Die_Temp_H	R	-	4 MSB of current die temperature in °C.

Table 20. Read Register – Operating Frequency

$$f_{OP}=\frac{64 * 6000}{OP\_FREQ\ [15:0]}$$

Address and Bit	Register Field Name	R/W	Default	Function and Description
48_{HEX} [7:0]	OP_FREQ[7:0]	R	-	8 LSB AC signal frequency on the coil.
49_{HEX} [7:0]	OP_FREQ[15:8]	R	-	8 MSB AC signal frequency on the coil.

Table 21. Alignment X Value Register

Note: Valid only in presence of the alignment PCB coil. (See section 8.10 or the *P9221-R Evaluation Kit User Manual* for more information.)

Address and Bit	Register Field Name	R/W	Default	Function and Description
$4B_{HEX}$ [7:0]	Align_X	R	-	8-bit signed integer representing alignment between TX and RX coil in the X-direction. The value is application-specific.

Table 22. Alignment Y Value Register

Note: Valid only in presence of the alignment PCB coil. (See section 8.10 or the *P9221-R Evaluation Kit User Manual* for more information.)

Address and Bit	Register Field Name	R/W	Default	Function and Description
$4C_{HEX}$ [7:0]	Align_Y	R	-	8-bit signed integer representing alignment between TX and RX coil in the Y-direction. The value is application-specific.

Table 23. Command Register

Address and Bit	Register Field Name	R/W	Default	Function and Description
$4E_{HEX}$ [7:6]	Reserved	R	0_{HEX}	Reserved.
$4E_{HEX}$ [5]	Clear Interrupt	RW	0_{HEX}	If application processor sets this bit to "1," the P9221-R clears the interrupt pin.
$4E_{HEX}$ [4]	Reserved	R	0_{HEX}	Reserved
$4E_{HEX}$ [3]	Send End of Power	RW	0_{HEX}	If application processor sets this bit to "1," the P9221-R sends the end power transfer packet (defined in the *End of Power Transfer* register shown in Table 15) to the transmitter and then sets this bit to "0."
$4E_{HEX}$ [2]	Reserved	R	0_{HEX}	Reserved
$4E_{HEX}$ [1]	Toggle LDO On/OFF	RW	0_{HEX}	If application processor sets this bit to "1," the P9221-R toggles the LDO output once (from on to off or from off to on), and then sets this bit to "0."
$4E_{HEX}$ [0]	Reserved	R	0_{HEX}	Reserved

12. Application Information

12.1 Power Dissipation and Thermal Requirements

The use of integrated circuits in low-profile and fine-pitch surface-mount packages requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks, convection surfaces, and the presence of other heat-generating components.

The P9221-R package has a maximum power dissipation of approximately 1.72W, which is governed by the number of thermal vias between the package and the printed circuit board. The die's maximum power dissipation is specified by the junction temperature and the package thermal resistance. The WLCSP package has a typical θ_{JA} of 47°C/W with 8 thermal vias and 77°C/W with no thermal vias. Maximizing the thermal vias is highly recommended. The ambient temperature surrounding the power IC will also have an effect on the thermal limits of the PCB design. The main factors influencing thermal resistance (θ_{JA}) are the PCB characteristics and thermal vias. For example, in a typical still-air environment, a significant amount of the heat generated is absorbed by the PCB. Changing the design or configuration of the PCB changes the overall thermal resistivity and therefore the board's heat-sinking efficiency.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design and improving the thermal coupling of the component to the PCB.
- Introducing airflow into the system.

First, the maximum power dissipation for a given situation should be calculated using Equation 3:

Equation 3

$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_A)}{\theta_{JA}}$$

Where

$P_{D(MAX)}$ = Maximum power dissipation

θ_{JA} = Package thermal resistance (°C/W)

$T_{J(MAX)}$ = Maximum device junction temperature (°C)

T_A = Ambient temperature (°C)

The maximum recommended junction temperature ($T_{J(MAX)}$) for the P9221-R device is 125°C. The thermal resistance of the 52-WLCSP package (AHG52) is nominally θ_{JA}=47°C/W with 8 thermal vias. Operation is specified to a maximum steady-state ambient temperature (T_A) of 85°C. Therefore, the maximum recommended power dissipation is

$P_{D(Max)}$ = (125°C - 85°C) / 47°C/W ≅ 0.85 Watt

All the above-mentioned thermal resistances are the values found when the P9221-R is mounted on a standard board of the dimensions and characteristics specified by the JEDEC 51 standard.

12.2 Recommended Coils

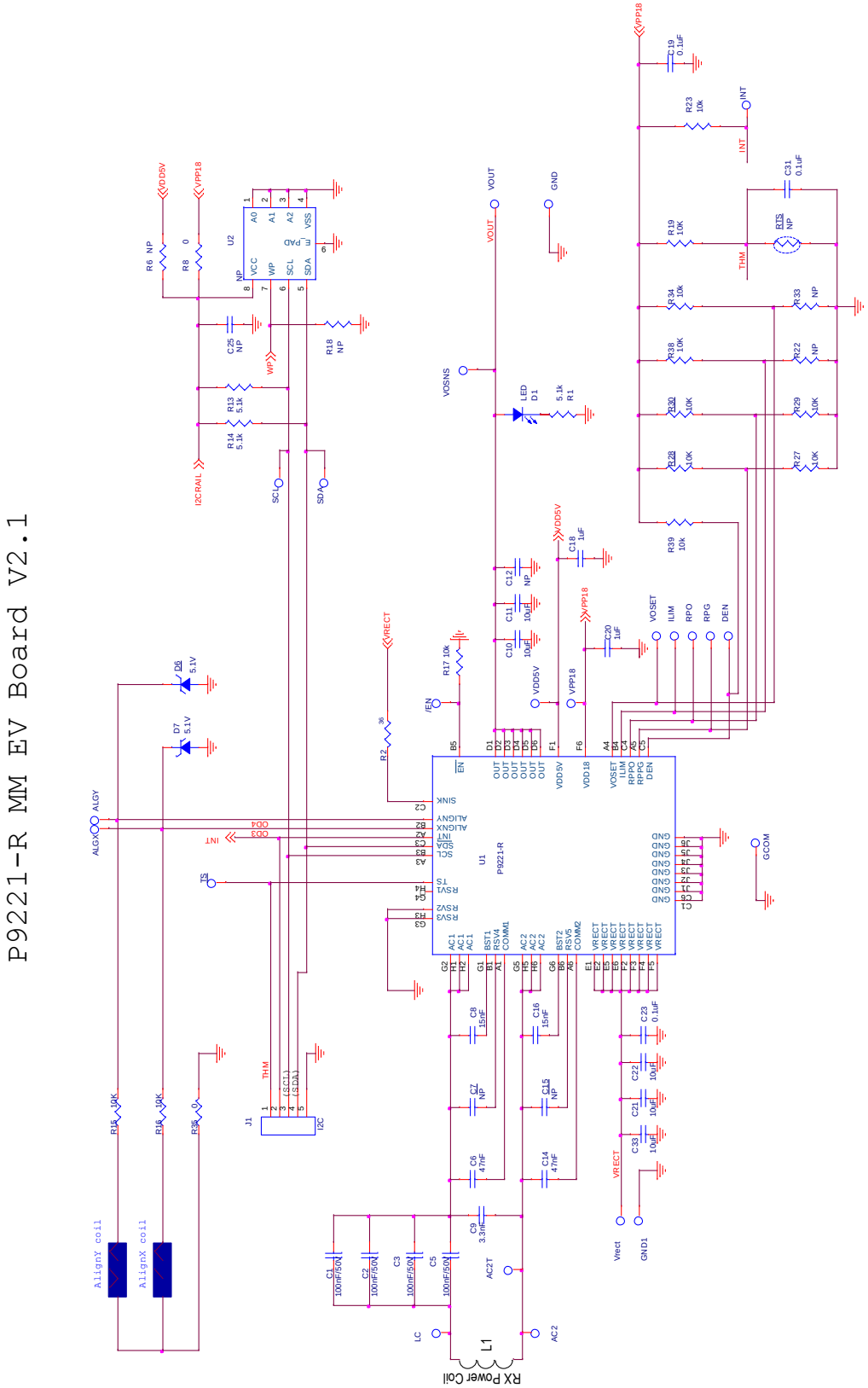
The following coil is recommended with the P9221-R receiver for 15W applications for optimum performance. The recommended vendor has been tested and verified.

Table 24. Recommended Coil Manufacturers

Output Power	Vendor	Part number	Inductance at 100kHz	ACR at 20°C
15W	AMOTECH	ASC-504060E00-S00	8.2µH	220 mΩ

12.3 Typical Application Schematic

Figure 24. P9221-R Typical Application Schematic



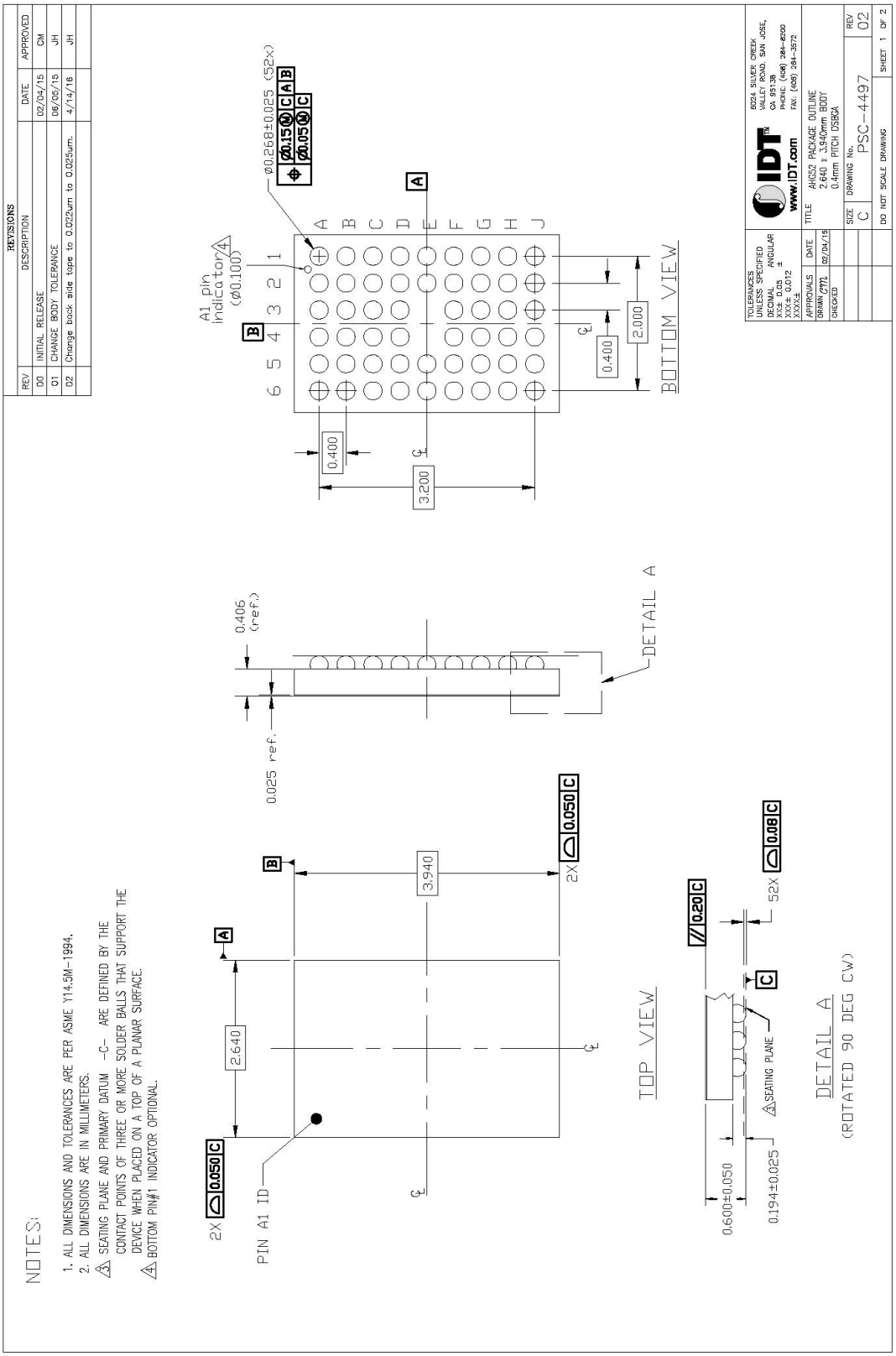
12.4 Bill of Materials (BOM)

Table 25. P9221-R MM Evaluation Kit V2.1 Bill of Materials

Item	Reference	Quantity	Value	Description	Part Number	PCB Footprint
1	AC2T, VDD5V, VPP18, VOSET, TS, SDA, SCL, RPO, RPG, INT, ILIM, GCOM, DEN, ALGY, ALGX, /EN	16	PTH_TP	Test Pad		10MIL_35PAD
2	AC2, LC	2	NP	Test Point		test_pt_sm_135x70
3	C1, C2, C3, C5	4	100nF/50V	CAP CER 0.1UF 50V X5R 0402	GRM155R61H104KE19D	402
4	C6, C14	2	47nF	CAP CER 0.047UF 50V X7R 0402	C1005X7R1H473K050BB	402
5	C7, C15	2	NP	CAP CER 0.047UF 50V X7R 0402	C1005X7R1H473K050BB	402
6	C8, C16	2	15nF	CAP CER 0.015UF 50V X7R 0402	GRM155R71H153KA12J	402
7	C9	1	3.3nF	CAP CER 3300PF 50V X7R 0402	CL05B332KB5NNNC	402
8	C10, C11, C21, C22, C33	5	10uF	CAP CER 10UF 25V X5R 0603	CL10A106MA8NRNC	603
9	C12	1	NP	CAP CER 10UF 25V X5R 0603	CL10A106MA8NRNC	603
10	C18	1	NP	CAP CER 1UF 10V X5R 0402	GRM155R61A105KE15D	402
11	C20	1	1uF	CAP CER 1UF 10V X5R 0402	GRM155R61A105KE15D	402
12	C19, C25, C31	3	0.1uF	CAP CER 0.1UF 10V X5R 0201	C0603X5R1A104K030BC	201
13	C23	1	0.1uF	CAP CER 0.1UF 25V X5R 0201	CL03A104KA3NNNC	201
14	D1	1	LED	LED GREEN CLEAR 0603 SMD	150060GS75000	0603_diode
15	D6,D7	2	5.1V	DIODE ZENER 5.1V 100MW 0201	CZRZ5V1B-HF	201
16	GND1, VRECT, VOUT, VOSNS, GND	5	Test Point	TEST POINT PC MINIATURE SMT	5015	test_pt_sm_135x70
17	L1	1	RX coil	AMOTECH, Rx Power Coil	ASC-504060E00-S00	10MIL_35PAD
18	J1	1	NP	HEADER_1X5_0P1PITCH60P42D	68002-205HLF	header_1x5_0p1Pitch60p42d
19	RTS	1	NP			NTC2
20	R1, R13, R14	3	5.1k	RES SMD 5.1K OHM 5% 1/16W 0402	MCR01MRTJ512	402
21	R2	1	36	RES SMD 36 OHM 5% 1/2W 0805	ERJ-P06J360V	805
22	R6	1	NP	RES SMD 0.0OHM 1/10W 0402	ERJ-2GE0R00X	402
23	R8	1	0	RES SMD 0.0OHM 1/10W 0402	ERJ-2GE0R00X	402
24	R15, R16	2	10K	RES SMD 10KOHM 1% 1/10W 0603	RC0603FR-0710KL	603
25	R17, R19, R23, R27, R28, R29, R30, R34, R38, R39	10	10k	RES SMD 10K OHM 5% 1/10W 0402	ERJ-2GEJ103X	402
26	R18, R22, ,R33	3	NP	RES SMD 10K OHM 5% 1/10W 0402	ERJ-2GEJ103X	402
27	R35	1	0	RES SMD 0.0OHM JUMPER 1/10W 0603	MCR03EZPJ000	603
28	U1	1	P9221-R	Wireless power receiver	P9221-R	csp52_2p64x3p94_0p4mm
29	U2	1	NP	IC EEPROM 128KBIT 400KHZ 8TDFN	24AA128T-I/MNY	TDFN08

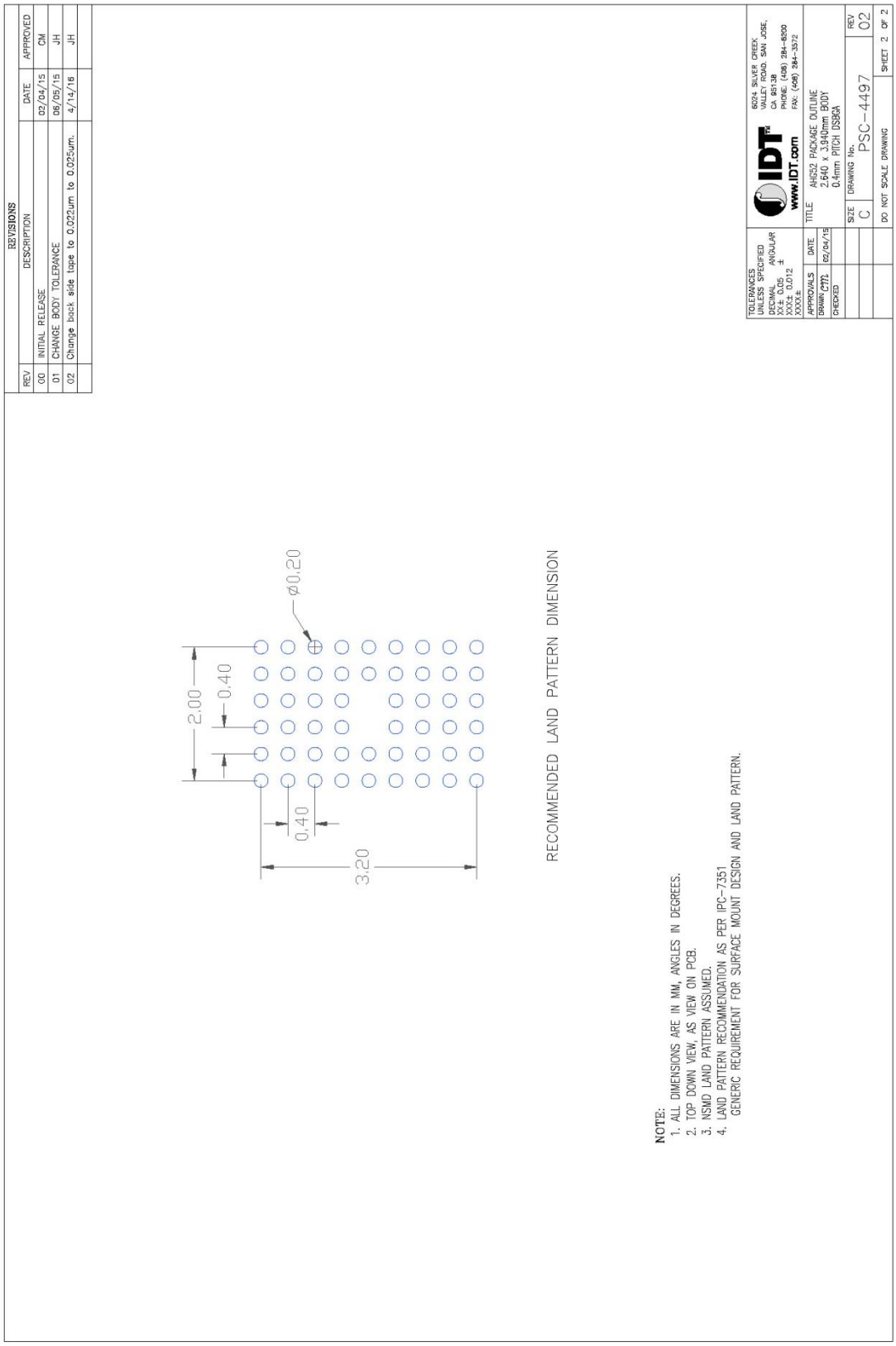
13. Package Drawings

Figure 25. Package Outline Drawing



14. Recommended Land Pattern

Figure 26. AHG52 52-WLCSP Land Pattern

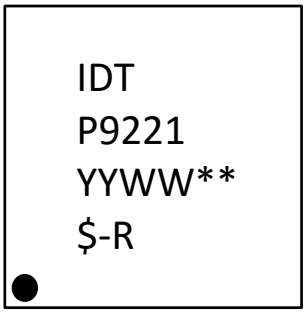


15. Special Notes: AHG52 WLCSP-52 Package Assembly

Unopened dry packaged parts have a one-year shelf life.

The HIC indicator card for newly-opened dry packaged parts should be checked. If there is any moisture content, the parts must be baked for a minimum of 8 hours at 125˚C within 24 hours of the assembly reflow process.

16. Marking Diagram



1. Line 1 company name.
2. Truncated part number.
3. “YYWW” is the last digit of the year and week that the part was assembled.
   ** is the lot sequential code.
4. “$” denotes mark code, -R is part of the device part number

17. Ordering Information

Orderable Part Number	Description and Package	MSL Rating	Shipping Packaging	Ambient Temperature
P9221-RAHGI8	P9221-R Wireless Power Receiver for 15W Applications, 2.64 × 3.94 mm 52-WLCSP (AHG52)	MSL1	Tape and reel	0°C to +85°C
P9221-R-EVK	P9221-R-EVK Evaluation Board			

18. Revision History

Revision Date	Description of Change
April 4, 2017	▪ Update to WPC-1.2.3 compliant ▪ Update for I^2C slave address = 61_{HEX} ▪ Update for device identification register ▪ Update for firmware revision number register ▪ Updates for Table 13 and Table 16. ▪ Update for recommended coil part number and related entry in BOM. ▪ Update for disclaimer ▪ Addition of R9221-R Evaluation Kit order code ▪ Minor edits
December 16, 2016	Preliminary release.

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