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Product Name : AMOTECH ESD SUPPRESSOR
Part No. : AIES 12 U 02 0R2

Top view	Bottom view
	

Rev. date : 2011. 03. 23



AMOTECH. CO. LTD.
17-2, JAMWON-DONG, SEOCHO-GU,
SEOUL, KOREA
TEL : 82-2-544-1351 FAX : 82-2-517-7183

개 발

품질보증

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1. Reversion History

Date	Content	Rev. no	Page
2011.03.23	Initial Version	0	

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2. Parts description

2.1 Introduction

AIES Series protect valuable high-speed data circuits from ESD damage without distorting data signals as a result of its ultra-low (0.15pF typical) capacitance.

2.2 Features

- Exceeds testing requirements outlined in IEC 61000-4-2
- Ultra low capacitance (0.15pF typ.)
- Very low leakage current
- Fast response time
- Bi-directional

3. Applications

3.1 General Description

AIES Series is specially designed to protect sensitive electronics from the threat of the electrostatic discharge (ESD). The product reacts almost instantly to the transient voltage and effectively clamps it to the low voltage for the duration of the ESD transient. The product uses voltage dependant variable materials that inherently produce low capacitance and very low leakage current. Thus the device is virtually invisible to the circuit during normal operational mode. It is especially transparent to the high-speed digital circuits due to the high off-state impedance and low capacitance. Signals are not distorted or disrupted as shown by extensive testing. Using this product ESD protection, devices maintain signal integrity of high-speed data signals while protecting the circuit from ESD. The nature of the material creates a bi-directional part, which means that only one device per surge path is required to provide complete ESD protection regardless of the surge polarity.

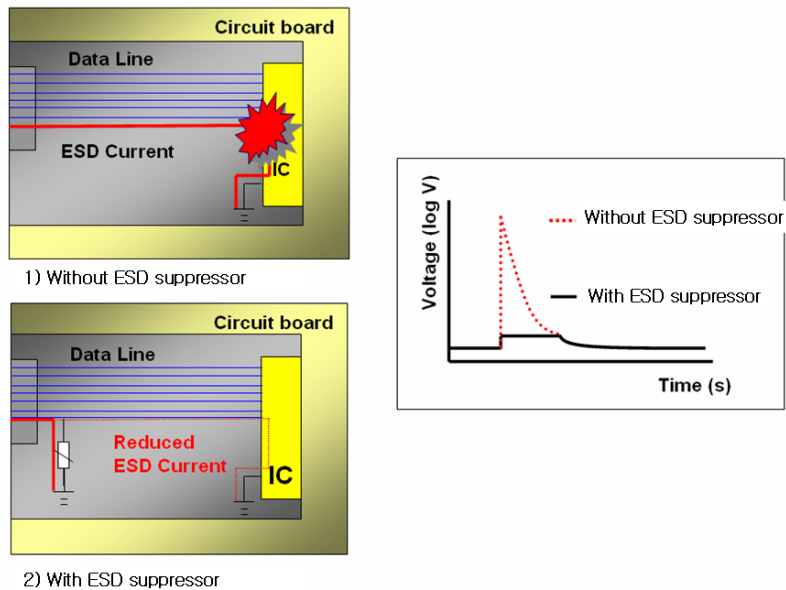
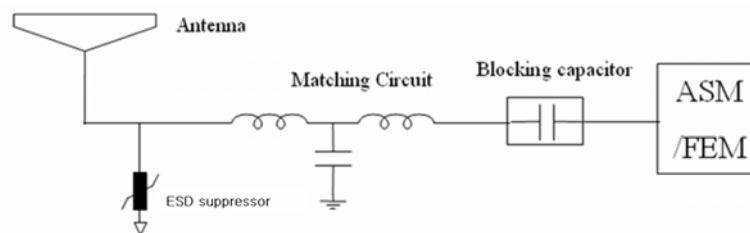


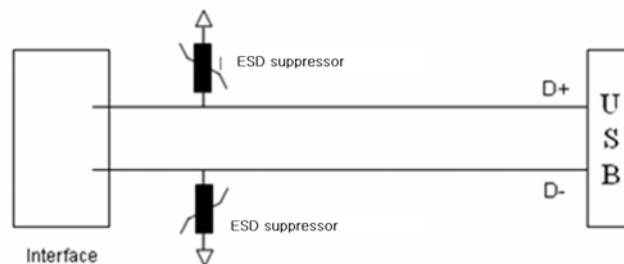
Fig 2) ESD Protection depending on the equipped ESD suppressor

3.2 Main application field

- ESD protection of SAW filter & diode switch in RF circuit
- ESD protection of USB 2.0 (high speed and full speed) circuit



(a) RF block



(b) USB block

Fig 3) Applied example in Mobile Phone.



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4. Model and Lot description system

Model : AIES 12 U 02 0R2
(1) (2) (3) (4) (5)

- (1) : Series name : **AIES** means **AMOTECH** Internal type **ESD** Suppressor.
- (2) : Rated voltage – Vdc: 12 means **12V**
- (3) : Capacitance Group: **U** means **Ultra** low capacitance
- (4) : Chip size: 02 means 0402 (1.0 x 0.5 mm)
- (5) : Capacitance : **0R2** means 0.2 pF

Lot : X 000 X X 00 X 00 XX
(1) (2) (3) (4) (5) (6) (7) (8)

- (1) : Display casting facility
- (2) : Ceramic Tape product #
- (3) : Display printing and stacking facility
- (4) : Display Product Type – P : Mass Production
- (5) : Produced year
- (6) : Produced Month ex) A : Jan. , B:Feb. ...
- (7) : Produced date
- (8) : Amotech Internal code

5. Specifications

5.1 Electrical characteristics

Characteristic	Value
Rated Voltage (Vdc)	12Vdc typ
Clamping Voltage ¹ (V _{C_ESD})	35typ, 50max
Capacitance (Cp, @ 1MHz)	0.15pF typ, 0.3pF max.
Leakage Current (IL, @ 12Vdc)	1 μ A max.
ESD Capability IEC61000-4-2 Direct Discharge IEC61000-4-2 Air Discharge	8kV typ. 15kV typ.
ESD Pulse Withstand ¹	>1,000 typ.
Operating Temperature	-40°C to +85°C

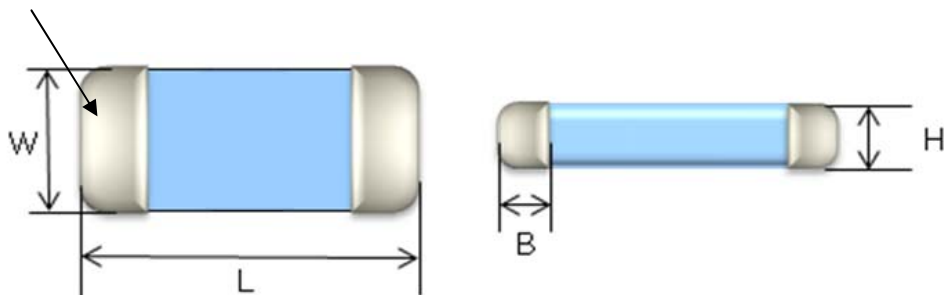
Notes

1 Per IEC61000-4-2, Level 4 waveform (8kV direct, 30A) measured 30ns after initiation of pulse.

5.2 Mechanical characteristics

- Appearance and dimension

Terminal Electrode



Symbol	L	W	H	B
Size (mm)	1.0±0.1	0.5±0.1	0.3±0.05	0.2±0.1



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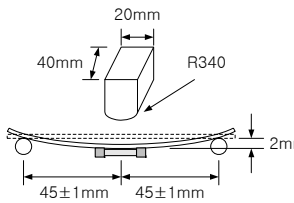
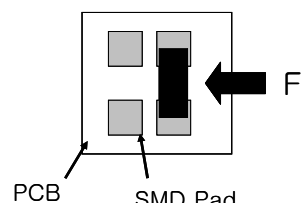
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6. Reliabilities and Test conditions

Parameter	Test	Test methods and remarks	Test requirement
Environmental reliability	ESD C=150 pF, R=330Ω	IEC 61000-4-2 1. ESD Level : ±8KV(Contact) , Interval : 1sec 2. Mode : Contact discharge(Level 4) 3. Method : Both 5 times in positive/negative direction	1. IL < 1 uA 2. No visible Damage.
	Thermal Shock	Condition for 1 cycle 1 step : Min. -40℃, 30±3 min. 2 step : Max. +125℃, 30±3 min. Number of cycles : 50 times Place for 48±2hrs at room temp. condition, then measure	1. IL < 1 uA 2. No visible Damage.
	Low temp. resistance	1. Temp. : -40 ± 5℃ 2. time : 1000 ± 24 hrs 3. Place for 24±2hrs at room temp. condition, then measure	1. IL < 1 uA 2. No visible Damage.
	High temp. resistance	1. Temp. : +125 ± 5℃ 2. Time : 1000 ± 24 hrs 3. Place for 24±2hrs at room temp. condition, then measure	1. IL < 1 uA 2. No visible Damage.
	High Temp. & Humidity resistance	1. Temp. : +85 ± 5℃ 2. Humidity : 85 ± 5 % RH. 3. Time : 1000 ± 24 hrs 4. Place for 24±2hrs at room temp. condition, then measure	1. IL < 1 uA 2. No visible Damage.

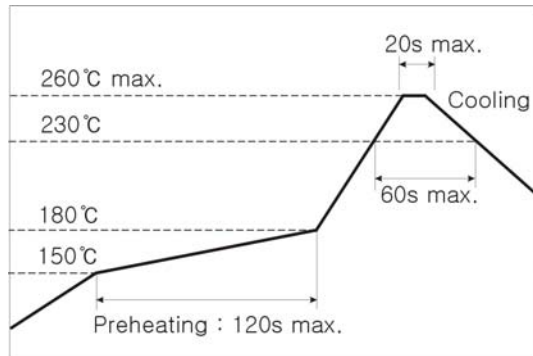
Parameter	Test	Test methods and remarks	Test requirement
Mechanical Reliability	Solderability	1. Test Machine : Solder Bath 2. Temp. : $245 \pm 5^{\circ}\text{C}$ 3. Time : 2s	At least 95% of terminal electrode is covered by new solder
	Resistance to soldering heat	1. Test Machine : Solder Bath 2. Temp. : $260 \pm 5^{\circ}\text{C}$ 3. Time : $10 \pm 0.5\text{s}$	1. IL < 1 uA 2. No visible Damage.
	Bending strength	1. Wrap: 2 mm 2. Speed: 0.5 mm/sec 3. Duration: 10sec  4. The measurement shall be made with board in the bent position	1. IL < 1 uA 2. No visible Damage.
	Adhesive strength	1. Applied force on SMD chip by fracture from PCB 	1. Strength > 0.8 Kgf (8N) 2. No visible Damage.

7. Soldering Condition

7.1 Soldering condition

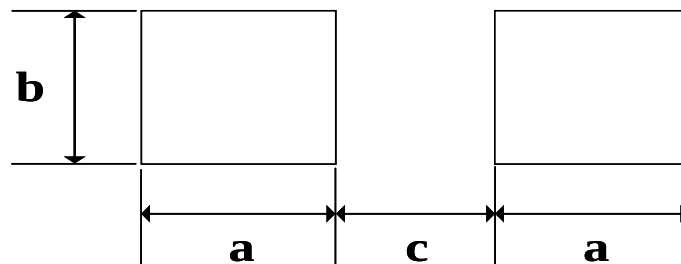
A. Lead Free Solder paste

Solder paste : Sn/Ag/Cu = 96.5/3.0/0.5



- Our chip suppressor are designed for reflow soldering only. Do not use flow soldering.
- Use non-activated flux (Cl content 0.2% max.).
- Follow the recommended soldering conditions to avoid varistor damage.

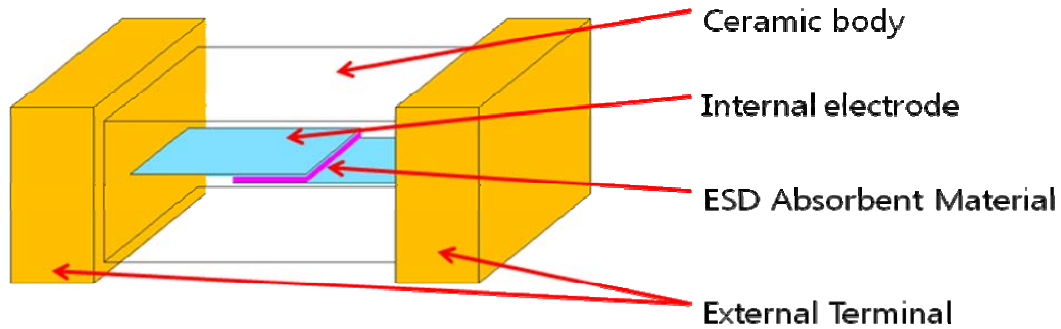
PCB pattern design condition (recommended)



Symbol	a	b	c
Size (mm)	0.4	0.6	0.64

8. Structure and Materials

8.1 Structure and materials specification



Item	Material specification
Ceramic Body	LTCC
Internal electrode	Ag
ESD absorbent	ZnO, Ag etc. Compound
External Terminal	Ag-Ni-Sn
Plating layer	Ni $\geq 1 \mu\text{m}$, Sn $\geq 2 \mu\text{m}$

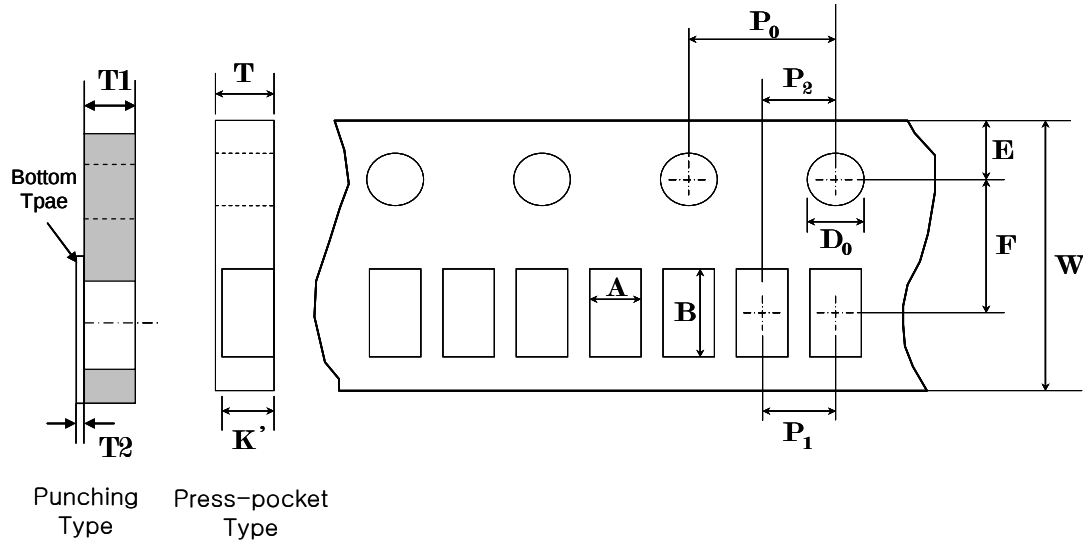
9. Cautions

1. Storage environment : -5~40℃ temperature, 70% humidity (MSL Level 1)
2. Do not use in high temperature/high humidity and a corrosive atmosphere like sulfide, chloride gas which could damage the solderability.
3. Do not expose ESD Suppressor to mechanical shock to avoid crack.
4. Use chips within 6 months. If over 6 months, check solderability before use.

10. Packaging specification

10.1 Carrier tape Specification

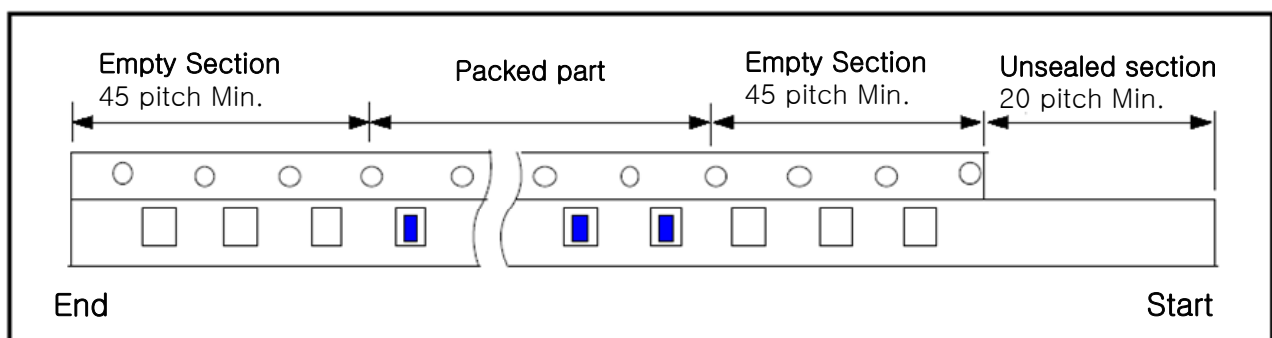
10.1.1 Size



(Unit :mm)

	A	B	D ₀	E	F	P ₀	P ₁	P ₂	W	K'	T	T1	T2
Spec.	0.62	1.12	1.55	1.75	3.50	4.00	2.00	2.00	8.0	0.60	0.65	0.60	0.1
Tolerance	± 0.04	± 0.04	± 0.10	± 0.05	± 0.05	± 0.10	± 0.05	± 0.05	± 0.1	± 0.03	± 0.03	± 0.05	Max

10.1.2 Chip Locations

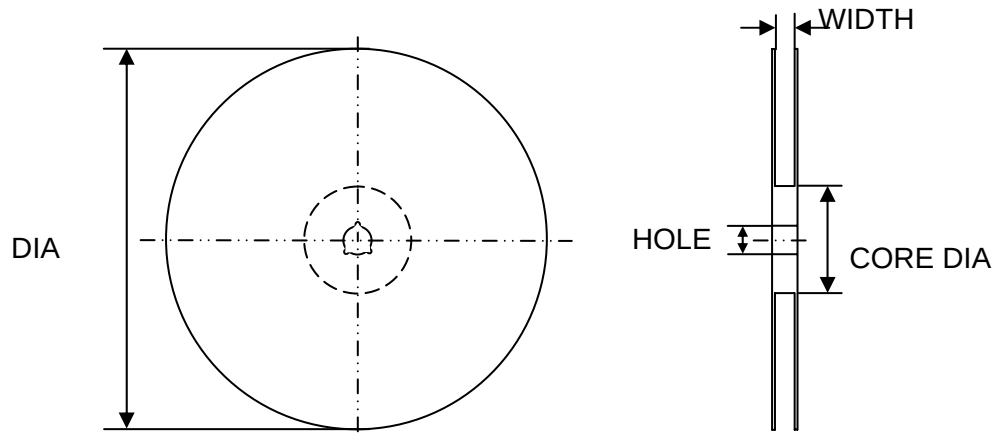


10.1.3 Materials

- 1) Paper carrier tape : Laminated virgin pulp
- 2) Top tape : Polyester film
- 3) Bottom tape : Adhesive coated paper

10.2 Reel Specification

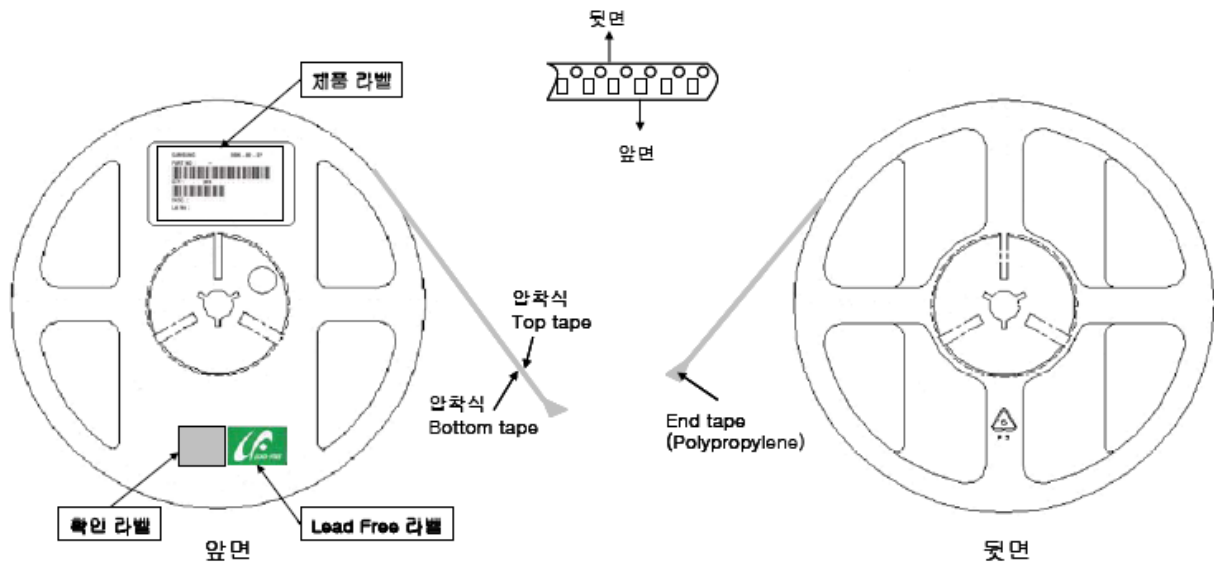
10.2.1 Size



unit : mm

	DIA	WIDTH	CORE DIA	HOLE
Size	178.0±0.5	9.0±0.5	60.0±1.0	13.2±0.3

10.2.2 Label adherence and winding direction



10.2.3 Material

- 1) Plastic reel : GPPS (General Purpose Poly Styrene) resin

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10.3 Box packaging Specification

10.3.1 Small Box

Size : 183 (W) x 185 (D) x 70 (T) (mm)

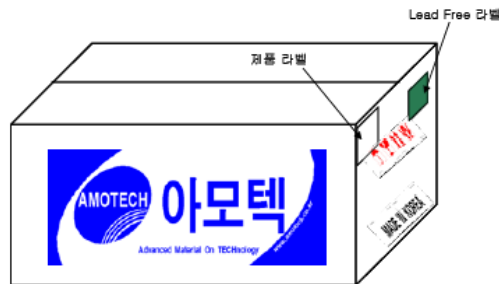
Quantity : 5 reel (10,000 ea/reel × 5 reel = 50,000 ea)



10.3.2 Medium Box

Size : 200 (W) x 375 (D) x 205 (T) (mm)

Quantity : 5 small boxes (50,000 ea/ small boxes × 5 small boxes = 250,000 ea)



10.3.3 Large Box

Size : 375 (W) x 390 (D) x 205 (T) (mm)

Quantity : 10 small boxes (50,000 ea/ small boxes × 10 small boxes = 500,000 ea)

